A Differential Implementation of the CMOS Active-Load Body-Effect Mixer

Thierry TARIS, Jean-Baptiste BEGUERET, Hervé LAPUYADE and Yann DEVAL

IXL Laboratory, University of Bordeaux, 351 cours de la libération, Talence, 33405, FRANCE

ABSTRACT — **This paper describes the implementation of a new mixer topology. The two input signals applied respectively to the back gate and the gate of two transistors achieve the mixing thanks to the active load body effect. The theoretical study of this effect is presented.**
Owing to the differential structure, the final circuit provides a conversion gain of more than 10 dB and reaches a 14 dB NF. The linearity is better than –5 dBm IIP3 while the architecture draws only 12 mW. Implemented in a 0.18µm CMOS VLSI technology, the circuit, dedicated to 3G mobile phone operates at 1.8V voltage supply.

I. INTRODUCTION

The demand for portable wireless communications systems is driven by the expansion of personal and commercial wireless services. As a result, the design of portable handsets follows trends that include lower cost, longer battery life, smaller size and lower weight. Thus this tendency disturbs the RFIC implementation that traditionally relies on bipolar or SiGe technologies for several gigahertz [1]. In fact these technologies well suited to achieve good analog features don't fill perfectly the needs of the mass market previously listed. At the same time, fine-line CMOS technologies continue to evolve as the demand for higher speed and more complex digital system grows while asserting itself in RF design too [2]. At present owing to the CMOS analog improvement and because of the mass market requirements VLSI technologies often replay bipolar ones in RF design blocks. However there is a major problem to be overcome, including the availability of on chip reliable passive components: the down scale supply voltage. Indeed closed to 1V it becomes difficult to provide good performances with traditional circuits. So that new topologies taking advantage of MOS transistor must be set up in order to overcome this constrain. In this paper a mixer available to operate under low voltage while maintaining good features is presented.

The theory of the body effect mixing with derived expressions is first presented. Then the 'active load body effect' concept fulfilling the drawbacks of the previous mixer brought into play previously is depicted with its own analytic expressions too. The third part describes the design of the implemented circuit followed by the experimental results.

II. BODY EFFECT MIXING

Body effect mixing is based on the fact that the substrate is modulated by a signal. Applying the latter to the bulk induces electron-hole pairs to flow from the channel to the bulk as depicted in Fig.1.

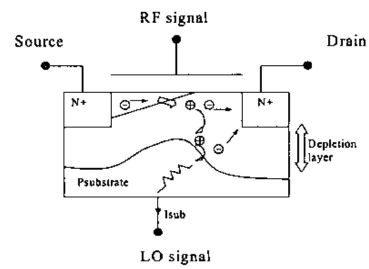

Fig1. Physical effect of body effect mixing

Due to the substrate width, these charges modulate the channel charge and thus the threshold voltage. This is known as the body effect and the expression of the threshold voltage V_T can be found in literature [3] as :

$$V_T = V_{T0} + \gamma\sqrt{2\varphi_F}\left[\sqrt{\left(1-\frac{V_{BS}}{2\varphi_F}\right)}-1\right]$$

With V_{T0} as the intrinsic threshold voltage, γ the body effect coefficient, φ_F the surface inversion potential of silicon and V_{BS} the bulk-source voltage.

Assuming $V_{BS} \ll 2\varphi_F$, applying the Taylor series to the previous expression leads to

$$V_T = V_{T0} + \gamma\sqrt{2\varphi_F}\left[\left(1-\frac{V_{BS}}{2.2\varphi_F}\right)-1\right]$$

And thus:

$$V_T = V_{T0} - \gamma\left(\frac{V_{BS}}{2.\sqrt{2\varphi_F}}\right)$$

so

$$V_T = V_{T0} + \alpha.V_{BS} \Rightarrow \alpha = -\frac{\gamma}{2.\sqrt{2\varphi_F}}$$

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This expression highlights a linear relationship between the threshold voltage of the NMOS transistor and the voltage potential applied on its bulk.

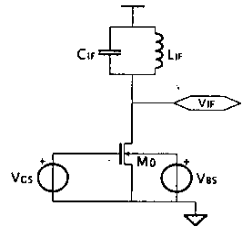

Fig2. The body effect mixing

The circuit depicted in Fig. 2 takes advantage of this principle to achieve a mixing operation [4].
Indeed, assuming M0 biased in the saturation region, it leads the expression of its drain current as following:

$$I_D = \frac{\mu_n C_{ox} W}{2L}(V_{GS} - V_T)^2$$

With μ_n as the electron mobility, C_{ox} the capacitance per unit area of the gate oxide, L and W respectively the NMOS length and width, V_{GS} the gate-source voltage and V_T the above mentioned threshold voltage.
Introducing the DC and alternative parts of V_{GS} and V_T signals as respectively V_{GS0} and ΔV_{GS} and V_{T0} and ΔV_T, as previously demonstrated, we have

$$\Delta V_T = \alpha V_{BS}$$

This leads to

$$I_D = \frac{\mu_n C_{ox} W}{2L}\left((V_{GS0} + \Delta V_{GS}) - (V_{T0} + \alpha V_{BS})\right)^2$$

so :

$$I_D = \frac{\mu_n C_{ox} W}{2L}\left[(V_{GS0} - V_{T0})^2 + 2(V_{GS0} - \Delta V_{T0})\right.$$
$$\left.(\Delta V_{GS} - \alpha V_{BS}) + (\Delta V_{GS})^2 + (\alpha V_{BS})^2 - 2\Delta V_{GS}\alpha V_{BS}\right]$$

The last term within the bracket confirms that the multiplication is completed by this circuit. Other products appear in the drain current, meaning that this mixer is not a four quadrant multiplier. However it is usually adequate to provide down conversion assuming that the LC tank load of M0 is tuned to the intermediate frequency. Thus, only taking into account the multiplication component of the drain current noted i_d :

$$i_d = -\frac{\mu_n C_{ox} W}{L}\left(\Delta V_{GS} \times \alpha V_{BS}\right)$$

Assuming that the RF signal is applied on the gate terminal such as

$$\Delta V_{GS} = V_{RF}\cos(\omega_{RF} t)$$

and that the local oscillator (LO) is applied on the bulk terminal, that is

$$V_{BS} = V_{LO}\cos(\omega_{LO} t)$$

It leads to the expression of i_d :

$$id = -\frac{\mu_n C_{ox} W}{2L}\alpha . V_{RF} . V_{LO}\left[\cos(\omega_{LO} + \omega_{RF}) + \cos(\omega_{LO} - \omega_{RF})\right]$$

Solely the (ω_{LO} - ω_{RF}) frequency lies within the bandwidth of the LC tank, yielding the intermediate frequency output voltage V_{IF} :

$$V_{IF} = \left[Z_{LC} \cdot \frac{\mu_n C_{ox} W}{2L}\alpha . V_{RF} . V_{LO}\right] . \cos(\omega_{LO} - \omega_{RF})t$$

with Z_{LC} the tank impedance.

This basic body effect mixer was first published in [4], and the theory was presented in [5]. The latter allows the designer to optimise the circuit to reach the highest conversion gain, as it emphasizes the influential parameters with regards to this gain. It appears that, among others, the local oscillator voltage amplitude has to be as large as possible for the circuit to act efficiently. On the other hand, M0 acts like a MOS capacitor having the local oscillator applied on one of its terminals while the RF input is applied on the other. The fact of the matter is that the local oscillator to RF isolation (LO-to-RF isolation) is too weak in this circuit, which is a major drawback from the receiver architecture laying emphasis to Direct Conversion Receiver (DCR).

III. THE MIXER PRINCIPLE

Fig. 3 represents the new mixer core. We still use the body effect to modulate M_{LO} but we apply RF to the other transistor. The PMOS is used to perform the body effect operation for the circuit to be VLSI compatible, avoiding expensive triple-well technologies.

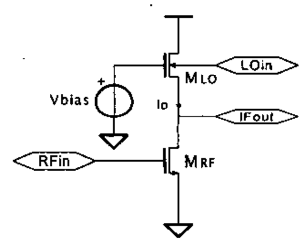

Fig3. The active load concept

Both M_{LO} and M_{RF} are active loads from each other, a topology denoted as the 'active load concept' [5]. The mixing principle is slightly different. Indeed, the I_D current in Fig. 3 can be expressed as follows :

$$\begin{cases} I_D = K_{RF}(V_{GSRF} - V_{TN})^2 . (1 + \lambda_N . V_{DSRF}) \\ I_D = K_{LO}(V_{GS0} - V_{TLO})^2 . (1 + \lambda_P . V_{DSLO}) \end{cases}$$

With K_{RF} and K_{LO} the transconductance parameters of respectively the NMOS and the PMOS transistors, V_{TN} and

V_{TLO} the threshold voltage of respectively the NMOS and the PMOS transistors, and λ_N and λ_P the channel length modulation parameters of respectively the NMOS and the PMOS transistors.

Assuming that the RF signal is applied on the M_{RF} gate terminal such as

$$V_{GSRF} = V_{GS0RF} + V_{RF}\cos(\omega_{RF}\, t)$$

And that the local oscillator (LO) is applied on M_{LO} bulk terminal, leading to

$$V_{TLO} = V_{TP} - \alpha V_{LO}\cos(\omega_{LO}\, t)$$

And emphasizing the V_{GSRF} times V_{TLO} multiplication in the drain current equation, we can write:

$$-V_{DSLO} = V_{DD} - V_{DSRF}$$

with V_{DSRF} equal to :

$$V_{DSRF} = \frac{1}{\lambda}\left(\frac{I_D}{K_{RF}(V_{GSRF} - V_{TN})^2} - 1\right)$$

Assuming $-\lambda_P = \lambda_N = \lambda$. V_{DSLO} is then introduced in I_D yielding:

$$I_D = K_{LO}.(2+\lambda.V_{DD}).(V_{GS0} - V_{TLO})^2$$

$$\frac{K_{RF}(V_{GSRF} - V_{TN})^2}{K_{RF}(V_{GSRF} - V_{TN})^2 + K_{LO}(V_{GS0} - V_{TLO})^2}$$

Under the assumption that alternative signals are weak compared to DC value, this current can be expressed as :

$$I_D \approx K_{LO}.(2+\lambda.V_{DD}).(V_{GS0} - V_{TLO})^2$$

$$\frac{K_{RF}(V_{GSRF} - V_{TN})^2}{K_{RF}(V_{GS0RF} - V_{TN})^2 + K_{LO}.(V_{GS0} - V_{TP})^2}$$

So,

$$I_D \approx K_{LO}.(2+\lambda.V_{DD}).(V_{GS0} - V_{TLO})^2$$

$$\frac{K_{RF}(V_{GSRF} - V_{TN})^2}{K_{RF}(V_{GS0RF} - V_{TN})^2 + K_{LO}.(V_{GS0} - V_{TP})^2}$$

The previous expression includes a lot of terms, among which is the multiplication term we are interested in. Focusing on the latter gives the intermediate frequency component noted i_D :

$$i_D \approx \frac{K_{RF}.K_{LO}.(2+\lambda.V_{DD})}{K_{RF}(V_{GS0RF} - V_{TN})^2 + K_{LO}.(V_{GS0} - V_{TP})^2}$$

$$(V_{GS0RF} - V_{TN}).(V_{GS0} - |V_{TP}|).(-\alpha V_{GS0} V_{TN}) \times V_{RF}.V_{LO}$$

$$\times \cos(\omega_{LO} - \omega_{RF})$$

So one can observe that the down-conversion is achieved.

IV. THE DESIGN

The circuit design is depicted in Fig 4, it can be separated in two parts:

The differential mixer core is built around the four transistors M_{RFi}, M_{LOi}. The principle has been described in the previous section. The 'active load concept' yields high gain, thus the Miller effect could cut off the mix. However, thanks to the feedback which holds on the output DC level and so improves the linearity, the parasitic problems are removed. We used a differential structure in order to improve the linearity and reduce substrate coupling effects. One can observe that an inductive degenerescence (L_{gi}, L_{si}) is used to optimize gain and noise figure regarding the RF port.

The common mode feedback is realized around a semidifferential pair which acts like a low pass filter thanks to the weak $(W/L)_{MFBi}$ ratio leading to weak biasing condition and thus low frequency cutoff. The two RC filters R_{out} coupled with C_{gs} and R_0,C_0 contribute to further cut off the high frequencies.

Dedicated to low voltage applications we decided not to stack more than two transistors between the supply rails. All the polarizations are external in order to test the architecture under different supply voltage 1.8V.

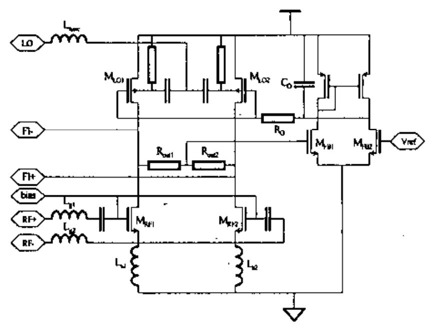

Fig4. the differential active load concept body effect mixer

IV. MEASUREMENT RESULTS

The chip micrograph is depicted in Fig. 5, the mixer size is 175µm*50µm.

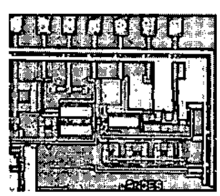

Fig5. chip micrograph

Implemented in a 0.18 µm CMOS VLSI technology the chip packaged in a ceramic JLCC 28 was soldered on a FR4 board routed with microstrip line coupled with ground filled area and the LO differential signal is provided by a resonator ring. Obviously these informations imply that an amount of signal is lost due to the test conditions. The power collect becomes very difficult on FR4 support in the 2 GHz range.

An excellent isolation of –52 dB between LO and RF ports is achieved thanks to the 'active load concept' that keeps the two input signals away from each other. The third section depicted that the higher the LO amplitude better the conversion gain so that one can enhance the last one without disturbing RF signal. This is a key behavior of mixers which target the low IF applications.

Providing a 10 dB of conversion gain collected via an active probe connected to a 40 GHz Agilent 8563E Spectrum Analyser the circuit takes advantage of the 'active load concept'. From the low voltage point of view, the topology provides a 3 dB conversion gain under 1.1 V with 4.5 mA current consumption. Under 1V the CMFB was out of range to enslave the DC voltage so that we couldn't extract meaningful features in this case.

When we design the circuit and choose the transistor size for noise optimization by inductive degenerescence [6] we decided to report the back gate noise to the noise input generators. Due to the low Q resonance of the inductance in frequency band of interest and the closeness of LO and RF frequencies we decided to calculate the values of the inductances at 2 GHz. According to the simulation this technique seems to be efficient for body effect noise calculating. In fact the 14 dB noise figure measured at the frequency of interest 190 MHz with a HP 8970B noise figure meter is closed to the 13 dB simulation result.

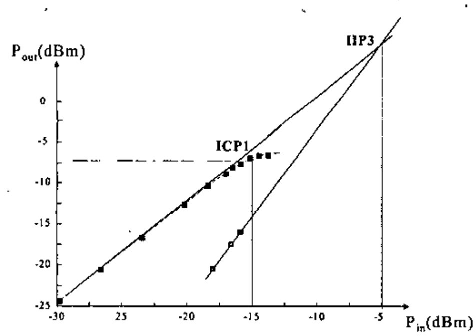

Fig 6. ICP1 and IIP3

Two design aspects lead to improve the linearity: first the differential structure and second the DC feedback. It holds on the output DC voltage and so the conversion gain feature that allows to extend the –1 dB compression point. Nevertheless due to it physical structure: long Pwell access, large inverted PN junctions, inverted doped structure, strong transversal field, many parasitic components compose the bulk port model. Thus these ones modify the shape of the LO signal and reduce the overall linearity of the circuit. However the –15 dBm ICP1 and –5 dBm IIP3 highlits the good behavior of the circuit from linearity point of view. The performance summary of the mixer is shown in table 1.

TABLE I
MEASUREMENT RESULTS

Voltage	1.8 V
Power consumption	12 mW
Conversion gain	10 dB
Noise figure	14 dB
ICP1	-15 dBm
IP3	-5 dBm
LO>RF isolation	-52 dB
LO frequency	2.2 GHz

6. CONCLUSION

A differential active load body effect mixer has been presented in this paper with it own theory, paving the way to the optimization of the circuit parameters. Demonstrating 14 dB noise figure and 10 dB gain the consumption is lower than 12 mW. Thanks to the active load body effect brought into play the isolation between LO>RF reaches –52 dBm that is an excellent value. With a ICP1 of –15 dBm this new topology available to operate under low voltage supply is well able to achieve down-conversion in modern RF receivers and, thanks to the VLSI CMOS technology it is dedicated to, this mixer is appropriated for future System On a Chip (SOC) implementation.

8. REFERENCES

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